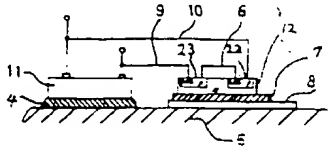
(54) SEMICONDUCTOR DEVICE
(11) 6-169057 (A) (43) 14.6.1994 (19) JP
(21) Appl. No. 5-185835 (22) 28.7.1993
(71) FUJI ELECTRIC CO LTD (72) TOSHIO SHIGEKANE
(51) Int. Cl⁵. H01L23/58,H01L27/04

PURPOSE: To provide a semiconductor device, wherein the overcurrent limit value becomes low when the bonding temperature of a transistor becomes high.

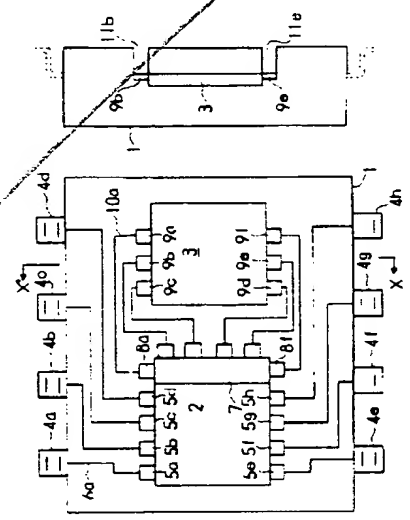
CONSTITUTION: Two diode parts 22 and 23 are constituted in one chip on a heat sink 5, to which a transistor chip 1 is fixed with a solder layer 4. A diode chip 12, which is connected in series with a lead wire 6 or a metal wiring, is fixed through an electrode plate 7 and an insulating ceramic plate 8. The transistor chip 11 and the diode chip 12 are connected with lead wires 9 and 10. When the diode chip 12 and the transistor chip 11 are close to each other and the insulating ceramic sheet plate 8 is thin or comprises ceramics having the excellent heat conductivity such as beryllium oxide, the bonding temperature of the transistor 11 and the bonding temperature of the diode 12 become approximately equal.



(54) SEMICONDUCTOR DEVICE
(11) 6-169058 (A) (43) 14.6.1994 (19) JP
(21) Appl. No. 4-319642 (22) 30.11.1992
(71) FUJITSU LTD (72) TAKASHI EBATO
(51) Int. Cl⁵. H01L25/04,H01L25/18,H01L21 66

PURPOSE: To perform the highly reliable test and evaluation, which sufficiently ensure the respective semiconductor chips even after packaging with regard to a semiconductor device, on which a plurality of semiconductor integrated circuit chips having the different functions are mounted on the same package.

CONSTITUTION: An active semiconductor integrated circuit chip (logic chip) 2 can send and receive the signals between the chip 2 and outer terminals 4 of a package 1. A passive semiconductor integrated circuit chip (memory chip) 3 does not have a means for sending and receiving signals between the chip 3 and the outer terminals 4 of the package 1, but sends and receives the signal only between the chip 3 and the active semiconductor integrated circuit chip 2. Dedicated testing terminals 11 for performing the test dedicated for the passive semiconductor integrated circuit chip 3 are provided in the package in the pattern so that the terminals 11 can be directly brought into contact with an electrode pads 9 of the passive semiconductor integrated circuit chip 3.

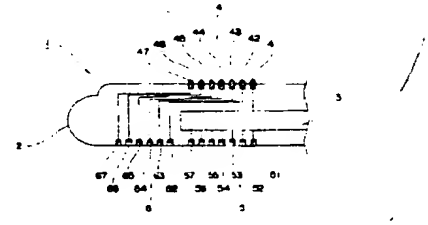


id: outer terminal 5a,8a,9a: pad, 6a,10a: lead

(54) COIN-TYPE INTEGRATED CIRCUIT
(11) 6-169059 (A) (43) 14.6.1994 (19) JP
(21) Appl. No. 4-345573 (22) 30.11.1992
(71) CASIO COMPUT CO LTD (72) KEIICHI KOBAYASHI
(51) Int. Cl⁵. H01L25/10,H01L25/11,H01L25/18

PURPOSE: To mount a plurality of groups in the laminated pattern in one containing part, which is provided in an electronic apparatus by providing a rear-side electrode groups, which are more than a surface-side electrode group by one group, on a substrate, connecting the first rear-side electrode group to an integrated circuit part in the substrate, and sequentially connecting the second and succeeding rear-side electrode groups to the surface-side electrode group.

CONSTITUTION: Concentric-circle-shaped electrode groups 4, 5 and 6 are provided on both upper and rear surfaces of an approximately coin-shaped substrate 2. First and second rear-side electrode groups 5 and 6, which are more than the surface electrode group 4 by one group, are set so that the positions of the groups 5 and 6 are made different in the direction of the diameter with respect to the surface-side electrode group 4. The first rear-side electrode group 5 is connected to an integrated circuit part (IC part) 3 in the substrate 2. The second and succeeding rear-side electrode groups 6 are sequentially connected to the surface-side electrode groups 4. Therefore, a plurality of the groups can be laminated and mounted in one containing part, which is prvided in an electronic apparatus. The upper-side coin-type integrated circuit 1 can be accessed through the second and succeeding rear-side electrode groups 6 and the surface-side electrode group 4, which is sequentially connected to the groups 6 at the lower-side coin-type integrated circuit 1, i.e., through electrodes 42-47.



coin-type integrated circuit
electrode